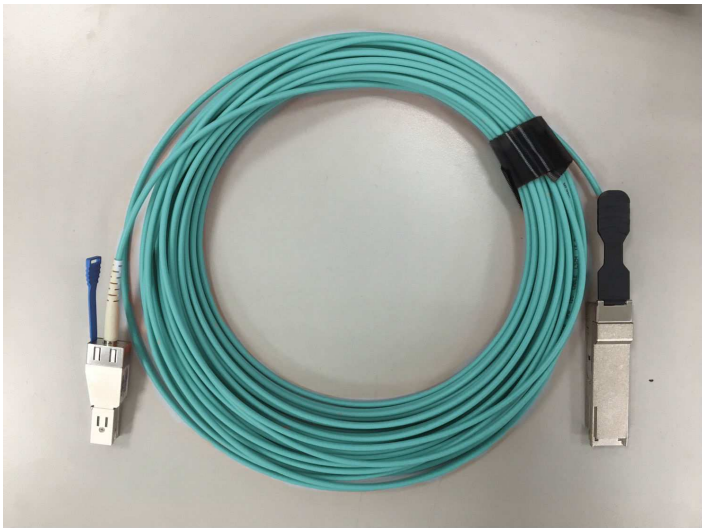
Specification

Small Form Factor Pluggable

Mini-SAS HD AOC Plug connect

Active Optical Cable

48 Gigabit Ethernet
Mini-SAS HD



TQS – 11E78 – JCAxx

Fiber Length

Model Name	Voltage	Category	Device type	Interface	LOS	Temperature
TQS-11E78-JCAxx	3.3 V	Without DDMI	VCSEL/PIN	AC/AC	CML/CML	+0°C~+70°C

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Purpose

This document validates solely for the product of Formerica Optoelectronics, 48-Gbps Mini-SAS HD to QSFP+ active optical cable (AOC) product specification. This document provides basic information and electronic characteristics for customer reference only, and subjects to change without notice.

General Description

Formerica's 48-Gbps Mini-SAS HD to QSFP+ AOC is of high-performance with full-duplex and aggregate 48-Gbps bandwidth for SAS-3 protocol specialized in storage applications. Compared with conventional copper cables, longer, lighter, and flexible AOCs enable the ease of complicated data-center cablings because of its small cable diameter of only 3-mm. High-quality 850-nm VCSELs and PIN PDs are utilized in this AOC cable with superior signal integrity and bit-error-rate (BER) performance, which enables reliable operation performance.
This 48-Gbps Mini-SAS HD AOC is compliant with SFF-8644 MSA with mechanical requirement, whose reduced size of connector provides premium board space for implementing more I/O ports. The single land speed is up to 12-Gbps to fulfill SAS-3 standard, also backward to fully compliant with SAS-2.1 of 6-Gbps land speed. Also, the out-of-band (OOB) low-speed hand-shaking communication is also supported with optical mold selection. This cable can be compliant to 40GBASE-SR4 Ethernet or 40-Gbps QDR InfiniBand protocol to meet several existing standards.

Feature

- Tx/Rx, Full-Duplex AOCs, Maximum aggregate speed of 48-Gbps for SAS3.0
- Backwards compatible to 6-Gbps SAS-2.1 of optical-mode capable systems with out-of-band (OOB) signal supported
- Bit-Error-Rate (BER) better than 10^{-12}
- Link length up to 100-m via OM3 MMF
- Round cable with small 3.0-mm outer diameter for flexible routing and easy cable management
- Compliant to SFF-8644 MSA standard in mechanical consideration
- Management interface compliant to SFF-8636
- QSFP+ to Mini-SAS HD AOC with different form-factors over two ends is available upon customer request

Absolute Maximum Rating

Not necessarily applied together. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Parameter	Min	Max	Unit	Note
Storage Temperature	-10	70	℃	1
3.3V Power Supply Voltage	-0.5	3.6	V	
Data Input Voltage- Single Ended	-0.5		V_{cc}+0.5	
Control Input Voltage	-0.5	3.6	V	
Relative Humidity	5	85	%	2

Notes:

1. Limited by the fiber cable jacket, not the active ends.
2. Non-condensing.

Recommended Operating Conditions

Parameter	Min	Typical	Max	Unit	Note
Case Operating Temperature	0	40	70	℃	
Power Supply Voltage	3.135	3.3	3.465	V	
Date Rate per Channel		12.0		Gbps	
Power Supply Noise Ripple Suscepti- bility (PSNR)			50	mV	1
Bit Error Ratio		10^{-12}			2
Control Input Voltage High	2		Vcc+0.3	V	
Control Input Voltage Low	-0.3		0.8	V	
Two Wire Serial (TWS) Interface Clock Rate		100		kHz	
Differential Data Input / Output Load		100		Ohms	
Standard Cable Lengths			100	m	3
Electrical Connector	Four-layers 36-pins			SFF-8644	
Management Interface	Two-Wire Serial			SFF-8636	

Notes:

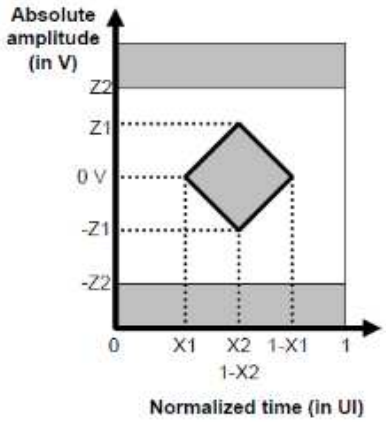
1. Power supply noise is defined as peak-to-peak noise amplitude over 1K to 15 MHz frequency range at host supply side by the recommended power supply filter for module. See Section 10 for the recommended power supply filter.
2. Bit-Error-Rate (BER) test can be compliant to SCRAMBLED_0 defined in Working Draft SAS Protocol Layer - 3 (SPL-3).
3. Longer cable length (up to 150-m via OM4) is available upon customer request.

Electrical Characteristics

Parameter	Min	Typical	Max	Unit	Note
Transceiver					
Transceiver Power Consumption for Mini-SAS HD End			1	W	
Transceiver Power Consumption for QSFP+ End			1.5	W	
Transceiver Power-On Initialization Time			2000	ms	1
Transmitter					
Maximum input peak to peak voltage (2× Z2)			1200	mVpp	2
Minimum input eye opening (2× Z1)	200			mVpp	2
Maximum half of TJ (X1)			0.175	UI	2
Maximum RJ			0.15	UI	2
Center of bit time (X2)		0.5		UI	2
Receiver					
Maximum output peak to peak voltage (2× Z2)			1200	mVpp	2
Minimum out eye opening (2× Z1)	360			mVpp	2
Maximum half of TJ (X1)			0.35	UI	2
Maximum RJ			0.45	UI	2
Center of bit time (X2)		0.5		UI	2

Notes:

1. "Initialization Time" is the time from when the supply voltages reach and remain above the minimum "Recommended Operating Conditions" to the time when the module enables TWS access. The module at that point is fully functional.
2. Refer to the 12Gbps active cable eye mask from SAS-3 working draft Rev. 06 (Nov. 7, 2013) of Figure 102 and Table 31.



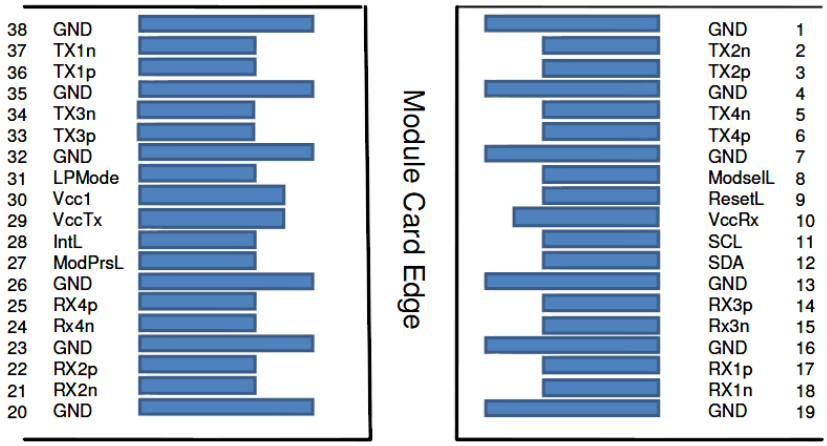
Optical Cable Specification

Parameter	Specification	Notes
Minimum Cable Bending Radius	30 mm	
Cable Cross-Section Dimension	Round Type Cable with 3 mm in Dia.	
Cable Cover Type	LSZH	1
Standard Cable Length	10, 20, 30, 50, 100-m	2
Cable Length Tolerance	+1.0 / -0 m	

Notes:
1. Cable cover type standard is LSZH. Other types can be available upon request.
2. Different cable length may be recommended to adopt different multi-mode fiber (MMF) grades of OM2, OM3, or OM4.

Connector Pad Assignments and Descriptions

The connector pad assignment of Mini-SAS HD to QSFP+ AOC is compliant to SFF-8449 and SFF-8436, respectively. The pad assignment and description is shown below.



Top Side
Viewed From Top

Bottom Side
Viewed From Bottom

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	2
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1

20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Notes:
1. GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2.. The connector pins are each rated for a maximum current of 500 mA.

Mini-SAS HD Connector Part (SFF-8644)

The Mini-SAS HD AOC plug connector is the 4 lane cable (free) connector defined in SFF-8644. The figure shows the appearance Mini-SAS HD cable plug connector.

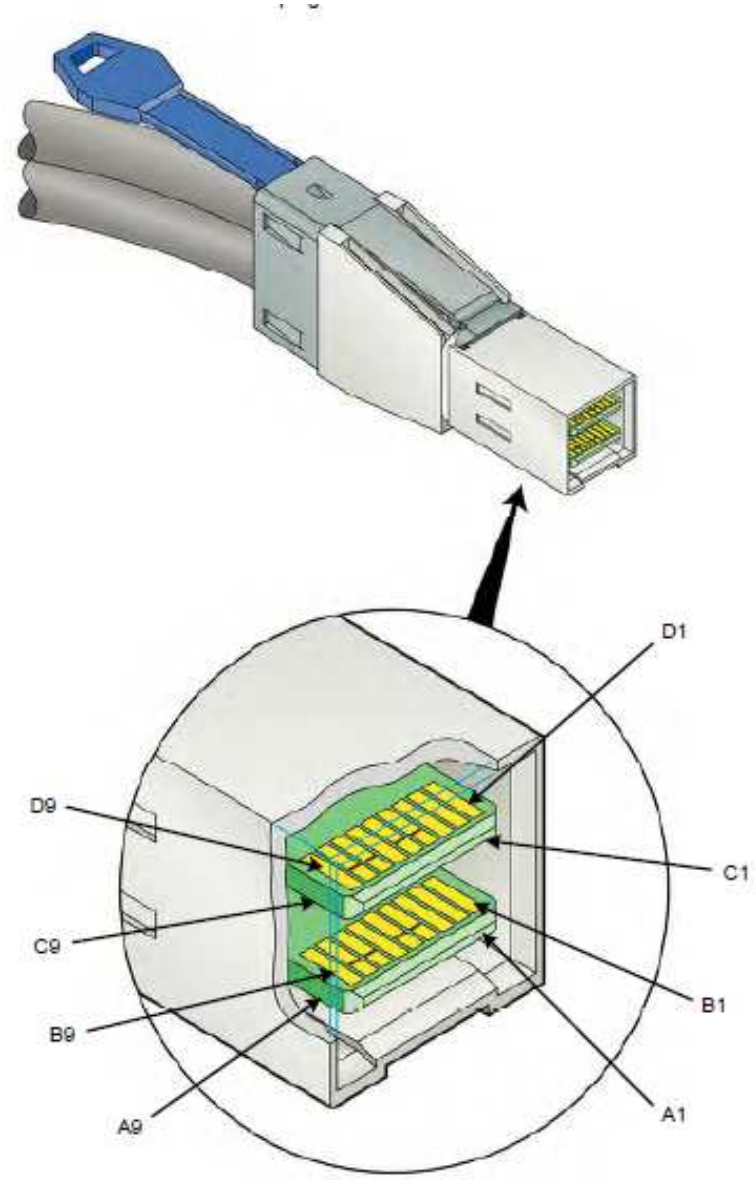


Fig. Mini-SAS HD AOC Plug connector

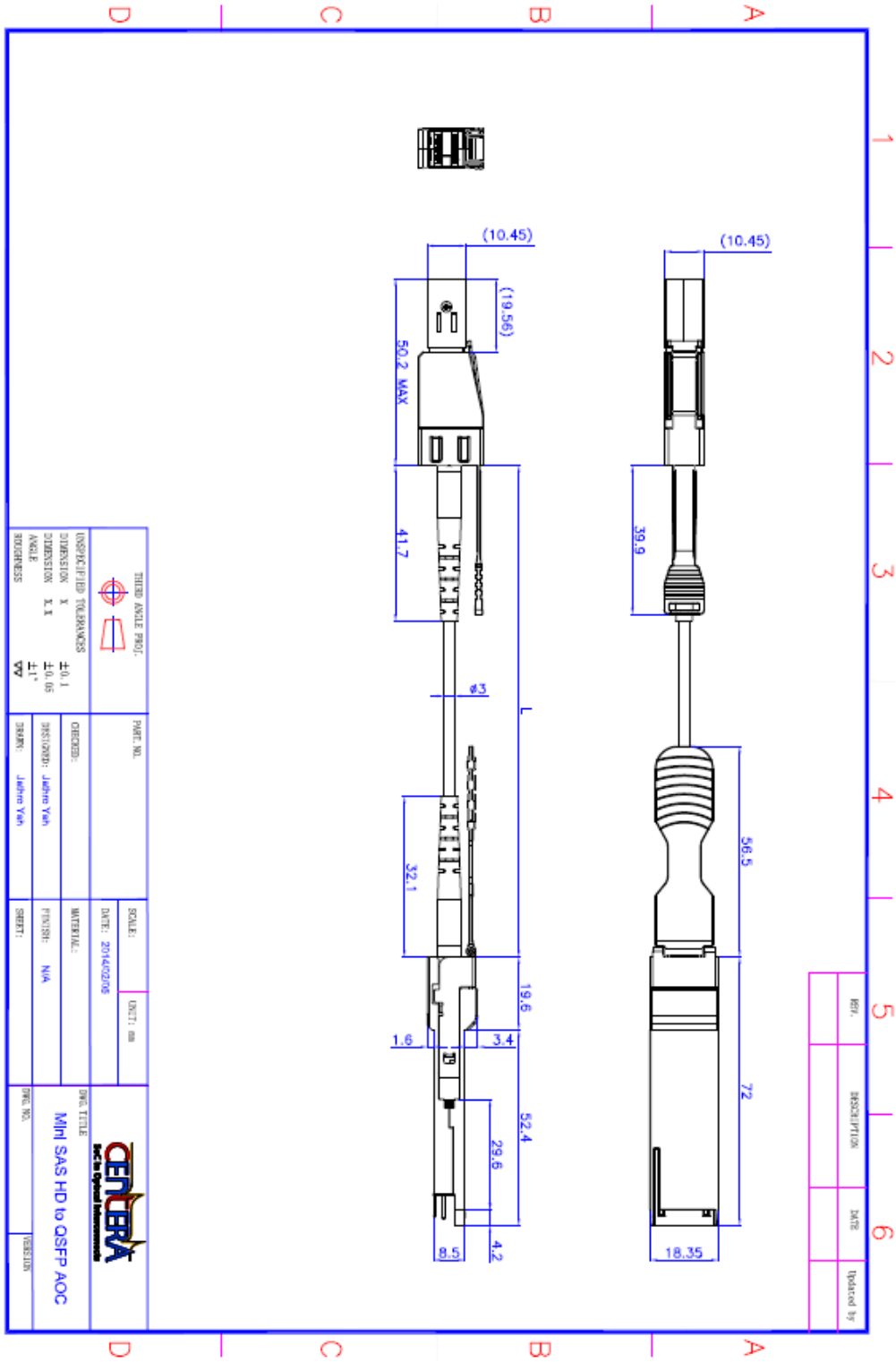
Tab. Mini-SAS HD Connector Physical Layer Interface

Signal	Pin	Mating Level	Definition
Reserved	A1	Second	Reserved for future use
IntL	A2	Second	Management interface interrupt signal
GND	A3	First	Signal ground
RX1+	A4	Third	Fixed side receiver channel 1 non-inverting input
RX1-	A5	Third	Fixed side receiver channel 1 inverting input
GND	A6	First	Signal ground
RX3+	A7	Third	Fixed side receiver channel 3 non-inverting input
RX3-	A8	Third	Fixed side receiver channel 3 inverting input
GND	A9	First	Signal ground
Vact	B1	Second	Free side power input for non-management interface circuitry
ModPrsL	B2	Second	Free side active low present output
GND	B3	First	Signal ground
RX0+	B4	Third	Fixed side receiver channel 0 non-inverting input
RX0-	B5	Third	Fixed side receiver channel 0 inverting input
GND	B6	First	Signal ground
RX2+	B7	Third	Fixed side receiver channel 2 non-inverting input
RX2-	B8	Third	Fixed side receiver channel 2 inverting input
GND	B9	First	Signal ground
SCL	C1	Second	Management interface serial clock
SDA	C2	Second	Management interface serial data output
GND	C3	First	Signal ground
TX1+	C4	Third	Fixed side transmitter channel 1 non-inverting output
TX1-	C5	Third	Fixed side transmitter channel 1 inverting output
GND	C6	First	Signal ground
TX3+	C7	Third	Fixed side transmitter channel 3 non-inverting output
TX3-	C8	Third	Fixed side transmitter channel 3 inverting output
GND	C9	First	Signal ground
Vact	D1	Second	Free side power input for non-management interface circuitry
Vman	D2	Second	Free side power input for management interface circuitry
GND	D3	First	Signal ground
TX0+	D4	Third	Fixed side transmitter channel 0 non-inverting output
TX0-	D5	Third	Fixed side transmitter channel 0 inverting output
GND	D6	First	Signal ground
TX2+	D7	Third	Fixed side transmitter channel 2 non-inverting output
TX2-	D8	Third	Fixed side transmitter channel 2 inverting output
GND	D9	First	Signal ground

Channel Assignment between QSFP+ and Mini-SAS HD

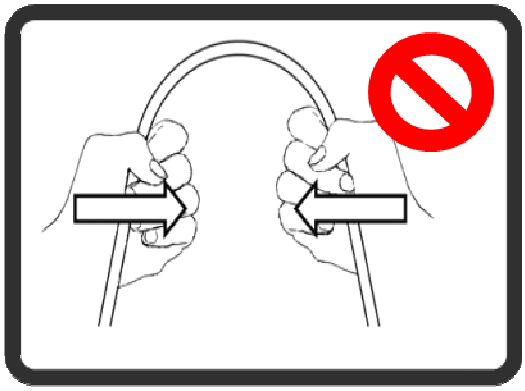
QSFP+ End	Signal Transmission Direction	Mini-SAS HD End
Tx1	→	Rx0
Tx2	→	Rx1
Tx3	→	Rx2
Tx4	→	Rx3
Rx4	←	Tx3
Rx3	←	Tx2
Rx2	←	Tx1
Rx1	←	Tx0

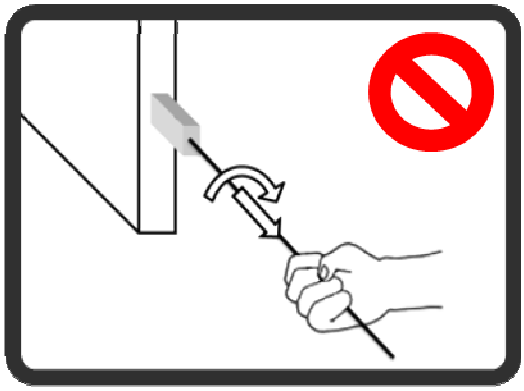
Mechanical Design Diagram



Handling

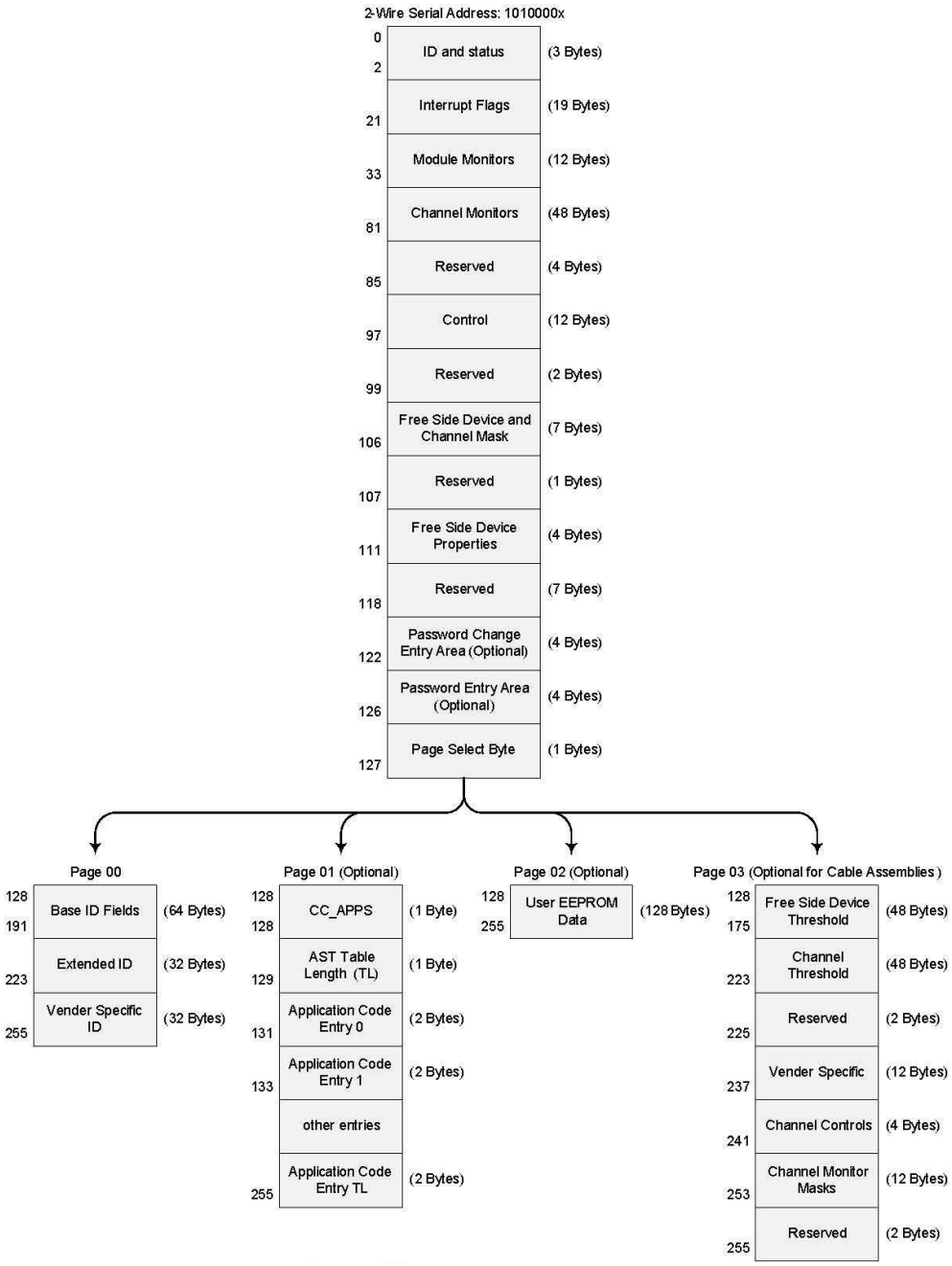
Care should be taken to restrict exposure to the conditions defined in the Absolute Maximum Ratings. Put the product in an even and stable location. If the product falls down or drops, it may cause an injury or malfunction. The cable must not be subject to extreme bends during installation or while in operation. If you bend the cable at a radius less than the cable minimum bend radius, then the cable may get damaged. Don't twist or pull by force ends of the cable, which might cause malfunction.





Memory Map

The memory map is structured as a single address and multiple page approaches, according to SFF-8636 MSA specification as shown in the below. For more detailed description of this memory map or lower pages, please see our Memory Map document with flexible customization settings.



Revision History

Date	Version	Description
03/06/2017	1.0	Initial release